**AMENDMENTS TO THE CLAIMS:**

*This listing of claims will replace all prior versions, and listings, of claims in the application:*

1. (*Currently amended*) A semiconductor device comprising:

a multi-layer SOI substrate comprising a first insulating layer, a first semiconductor layer, a buried insulating film, and a second semiconductor layer stacked in this order on a support substrate;

a first MOS transistor formed on and in [[a]] the second semiconductor layer of ~~an~~ the SOI substrate; ~~in which the semiconductor layer is formed on a semiconductor substrate of a first conductivity type with the intervention of a buried insulating film,~~

a contact portion for applying to the first semiconductor layer of the multi-layer SOI substrate ~~substrate~~ different bias voltages in an operating state and a standby state of a semiconductor circuit including the first MOS transistor,

the first MOS transistor including source and drain regions of a second conductivity type, a channel of the first conductivity type, and wherein an impurity diffusion layer of the first conductivity type is formed in the first semiconductor layer of the multi-layer SOI substrate ~~substrate~~ under at least the entire source, drain and channel regions, so that the impurity diffusion layer is of the same conductivity type as the first semiconductor layer of the multi-layer SOI substrate, ~~substrate~~ wherein said source and drain regions as well as said channel are all formed in the second semiconductor layer of the multi-layer SOI substrate;

wherein the contact portion for applying the different bias voltages is formed in a device isolation region and comprises a contact hole in the second semiconductor layer and the buried insulating film, said contact hole reaching the impurity diffusion layer so that the different bias

voltages are applied to the SOI substrate via the impurity diffusion layer, and wherein a conductor of the contact portion in the contact hole is electrically insulated from the second semiconductor layer by at least said device isolation region which includes at least one insulator;

a second MOS transistor, wherein the first and second MOS transistors are of different conductivity types on the SOI substrate and are adjacent each other, and wherein bias voltages applied via said contact portion for the first transistor and a contact portion for the second transistor are changed between the active and standby states so that active regions of the first and second transistors are substantially completely depleted ~~simultaneously~~ in the standby state; and

wherein the first MOS transistor comprises a P-type well and the second MOS transistor comprises an N-type well formed in the first semiconductor layer of the multi-layer SOI substrate ~~substrate~~, and wherein the P-type well of the first MOS transistor and the N-type well of the second MOS transistor are substantially electrically isolated from each other, and wherein the impurity diffusion layer makes up at least part of the P-type well of the first MOS transistor.

2-3. (*Canceled*)

4. (*Currently amended*) A semiconductor device according to claim 1, wherein the impurity diffusion region is formed as a well in a surface of the first semiconductor layer of the multi-layer SOI substrate ~~substrate~~ which lies under the first MOS transistor, the well having an impurity concentration higher than that of the other region of the first semiconductor layer. ~~substrate, and the bias voltages are applied to the well.~~

5. (*Currently amended*) A semiconductor device according to claim 4, wherein the well is a P-type well under an N-channel MOS transistor which is the first of said first and second MOS transistors, while a well for the other of the first and second MOS transistors is an N-type well formed in the first semiconductor layer ~~substrate~~ under a P-channel MOS transistor which is the second of said first and second MOS transistors.

6. (*Canceled*)

7. (*Currently amended*) A semiconductor device comprising:

a multi-layer SOI substrate comprising a first insulating layer, a first semiconductor layer, a buried insulating film, and a second semiconductor layer stacked in this order on a support substrate;

a first MOS transistor formed on and in [[a]] the second semiconductor layer of [[an]] the multi-layer SOI substrate ~~in which the semiconductor layer is formed on a semiconductor substrate with the intervention of a buried insulating film~~,

an element isolating region formed in the second semiconductor layer,

a contact region formed in the element isolating region for connection with a contact portion for applying a bias voltage to a well of the first semiconductor ~~substrate~~ layer of the multi-layer SOI substrate for the first MOS transistor, the well being of the first conductivity type same as that of the other region of the first semiconductor ~~substrate~~ layer of the multi-layer SOI substrate directly under the well;

wherein a conductor of the contact portion in the contact region is electrically insulated from said second semiconductor layer;

a second MOS transistor, wherein the first and second MOS transistors are of different conductivity types on the SOI substrate, and wherein bias voltages applied via said contact portion for the first transistor and a separate contact region including a contact portion for the second transistor are changed between the active and standby states so that active regions of the first and second transistors are substantially completely depleted ~~simultaneously~~ in the standby state; and

wherein the first MOS transistor comprises a P-type well and the second MOS transistor comprises a N-type well formed in the first semiconductor ~~substrate~~ layer of the multi-layer SOI substrate, and wherein the P-type well of the first MOS transistor and the N-type well of the second MOS transistor are substantially electrically isolated from each other.

8. (*Currently amended*) A semiconductor device according to claim 7, wherein the well is formed in a surface of the first semiconductor layer ~~which lies~~ under the first MOS transistor formed on the second semiconductor layer, the well having an impurity concentration higher than that of the other region of the first semiconductor layer. ~~substrate, and the bias voltages are applied to the well.~~

9. (*Currently amended*) A semiconductor device according to claim 8, wherein the well is a P-type well under an N-channel MOS transistor which is the first of said first and second MOS transistors, while a well for the other of the first and second MOS transistors is an N-type well formed in the first semiconductor ~~substrate~~ layer of the multi-layer SOI substrate under a P-channel MOS transistor which is the second of said first and second MOS transistors.

10. (*Canceled*)

11. (*Previously presented*) A semiconductor device according to claim 7, wherein different values of said bias voltages are applied in an operating state and a standby state of a semiconductor circuit including the at least the first MOS transistor, thereby to change a threshold voltage of at least the first MOS transistor.

12-23. (*Canceled*)

24. (*Currently amended*) A semiconductor device comprising:

a multi-layer SOI substrate comprising a first insulating layer, a first semiconductor layer of a first conductivity type, a buried insulating film, and a second semiconductor layer stacked in this order;

a PMOS transistor and an NMOS transistor formed on and in [[a]] the second semiconductor layer of [[an]] the SOI substrate ~~in which the semiconductor layer is formed on a semiconductor substrate of a first conductivity type with the intervention of a buried insulating film~~,

a p-type well formed in the first semiconductor layer of the SOI substrate for the NMOS transistor and an n-type well formed in the first semiconductor layer of the SOI substrate for the PMOS transistor, the p-type and n-type wells being substantially isolated from one another; and

respective contact portions for applying to the first semiconductor ~~substrate~~ layer of the multi-layer SOI substrate via the wells different bias voltages in a transistor operating state and a transistor standby state so that active regions of the different conductivity type transistors are

substantially completely depleted ~~simultaneously~~ in the standby state, wherein said contact portions are electrically insulated from said second semiconductor layer.